

Abstract of the Disclosure

A memory device includes an array of memory cells arranged in rows and columns with a portion of the rows of the memory cells being divided into segments. A global bias circuit generates a plurality of first bias currents. Each of a plurality of local bias networks includes a local bias circuit that generates a plurality of second bias currents in response to a corresponding one of the plurality of first bias currents, and includes a plurality of segment bias circuits that each generates a third bias current. Each segment bias circuit is adjacent to a corresponding segment of the memory cells. Each segment bias circuit provides a ground feedback signal to the local bias circuit, which adjusts the second bias current in response to the ground feedback signal. The segment bias circuits are disposed in geometric positions in the segments, which may be approximately one-fourth of the distance of the segments and relative to an end of the segment having the highest voltage drop or divide the bias voltage difference in the segment approximately equally. The global bias circuit includes a port for monitoring read current or altering write current. The memory device also includes a noise tolerant low voltage transceiver coupled between the bias circuits and a test pad.

TENTATIVE PRIORITY CLAIM